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IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Claim 1 (Currently amended): A data processing arrangement comprising:

a first processor for providing successive sets of input data;

a second processor for receiving successive sets of output data;

a memory system including a plurality of memory circuits where all of the plurality of memory circuits are accessible by the first processor for writing and all of the plurality of memory circuits are accessible by the second processor for reading;

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a master controller for setting up the plurality of memory circuits of said memory system using control commands associated with a set of input data and a set of output data; and

a control unit including at least two counters that can be externally loaded with variable, non-zero values, respectively, by signals from the first and second processors, the control unit, on the basis of the control commands and the signals, controls access to the memory system by the first and second processor in an asynchronous manner.

Claim 2 (Previously presented): A data processing arrangement, as claimed in claim 1, wherein the at least two counters includes:

a write-counter whose value is modified in association with the data received from the set of input data and which value indicates the write-address of the data in the first memory circuit; and

a read-counter whose value is modified in association with the data provided from the set of output data and which value indicates the read-address of the data in the second memory circuit.

Claim 3 (Previously presented): A data processing arrangement, as claimed in claim 1, wherein the control unit includes a write-input port for receiving a write-data signal from the first processor in response to which the control unit generates the write-address and the control unit further comprises a read-input port for receiving a read-data signal from the second processor in response to which the control unit generates the read-address.

Claim 4 (Currently amended): A memory system comprising:

a plurality of memory circuits for receiving successive sets of input data and for providing successive sets of output data, all of the plurality of memory circuits being accessible by at least one processor for writing and by at least another processor for reading;

a control unit including

at least two counters that can be externally loaded with variable, non-zero values, respectively, by signals from the at least two processors, and being programmable by means of control commands and the signals, and

a comparator for preventing the at least one processor for writing and the at least another processor for reading from accessing an identical respective one of the plurality of memory circuits simultaneously,

controls access to the plurality of memory circuits by the at least two processors in an asynchronous manner.

Claim 5 (Currently amended): A method of processing data in a data processing arrangement including a first processor for providing successive sets of input data, a second processor for receiving successive sets of output data and a memory system including a plurality of memory circuits that are all accessible by the first processor for providing the successive sets of input data and by the second processor for receiving the successive sets of output data, the method comprising, for a set of input data and a set of output data, the following steps:

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a configuration step in which the memory system is set up by means of control commands associated with the set of input data and the set of output data, the control commands selecting amongst a plurality of predefined addressing options;

a counter set-up step in which at least two counters receive ~~step-up~~set-up signals, respectively, from the first and second processor; and

an execution step in which, on the basis of the control commands and the step-up signal, the memory system:

controls access to the plurality of memory circuits by the first and second processors in an asynchronous manner.